218008US-2 CONT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

SHIGERU HASEGAWA :

SERIAL NO: NEW APPLICATION : ATTN: APPLICATION BRANCH

FILED: HEREWITH :

FOR: INSULATING GATE TYPE
SEMICONDUCTOR DEVICE

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to a first examination on the merits, please amend the above-identified application as follows:

IN THE CLAIMS

Please cancel Claims 1-6, 9, and 10 without prejudice.

Please amend Claim 7 as follows:

7. (Amended) An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof;

a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate and each recessed at a first distance (L5) and a second distance (L6) alternately, lower ends of said trenches extending to a depth extending from the surface of said semiconductor substrate to an upper portion of said N-type base layer;

a gate oxide layer provided on an inner surface of each of said trenches and on the surface of said semiconductor substrate;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate oxide layer and connected to said gate wire, with one set of said trench gate electrodes being constituted by twos arranged in sequence at the first distance (L5), and said first distance (L5) is greater than said second distance (L6);

an N-type emitter layer provided in the surface part of said P-type base layer having a length of said second distance (L6) interposed between said trench gate electrode belonging to said one set of electrodes and said trench gate electrodes belonging to another set of electrodes adjacent to said one set of electrodes, and in the vicinity of said trench gate electrode;

an insulating oxide layer provided covering a part or the whole of said trench gate electrode, and holed with contact holes at each of portions provided with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating oxide layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode provided on said P-type emitter layer on the underside of said semiconductor substrate;

wherein the predetermined depth of the trench is set to such an extent that a depletion layer formed extending from a top of said trench gate electrode when in a forward voltage application is fused with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is

vicinal and that a curvature of said depletion layer at the top of said trench gate electrode is relieved.

Please add new Claims 11-14 as follows:

11. (New) An insulating gate type semiconductor device according to Claim 7, wherein the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3 μm or less.

12. (New) An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof;

a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate, said plurality of trenches constituting a set of trenches, each set of trenches being disposed at an interval having a first distance (L5), each of said set of trenches having a second distance (L6) between both end trenches, and said first distance (L5) is greater than said second distance (L6);

an N-type emitter provided in the surface part of said P-type base layer having a width of the second distance;

a gate oxide layer provided at least on an inner surface of each of said trenches;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate oxide layer and connected to said gate wire;

an insulating oxide layer provided covering said trench gate electrode, and holed with contact holes at each of portions with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating oxide layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode provided on the underside of said P-type emitter layer,

wherein lower ends of said trenches extending to a depth from the surface of said semiconductor substrate to an upper portion of said N-type base layer to such an extent that a depletion layer formed extending from a tip of said trench gate electrode when in a forward voltage application is fused with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is vicinal and that a curvature of said depletion layer at the tip of said trench is relieved.

13. (New) An insulating gate type semiconductor device according to claim 12, wherein the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3 μm or less.

14. (New) An insulating gate type semiconductor device according to claim 12, wherein said insulating oxide layer is provided on the part of whole surface of said trench gate electrodes on said P-type base layer between a set of trenches and a next set of trenches.

REMARKS

Favorable consideration of this application, in view of the following comments and as presently amended, is respectfully requested.

The present application is a continuation of copending parent U.S. Application Serial No. 09/314,115.

In that parent application Claims 7, 8, and 11 were rejected under 35 U.S.C. §103(a) as unpatentable over U.S. patent 6,060,747 to Okumura et al. (herein "Okumura"), in view of Kitagawa et al., "A 4500V Injection Enhanced Insulated Gate Bipolar Transistor (IEGT) Operating in a Mode Similar to a Thyristor" (herein "Kitagawa").

To promote prosecution of the above-identified parent application, Claims 7, 8, and 11 were canceled.

The present new Continuation application and Preliminary Amendment are submitted to continue the prosecution of Claims 7, 8, and 11 cancelled in the parent of the present application, and to also set forth new Claims 12-14 for examination.

Each of the pending claims is believed to patentably distinguish over the teachings of Okumura in view of Kitagawa.

It is first noted that Claim 7 has been amended to clarify features recited therein.

First, Claim 7 recites "a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate". New independent Claim 12 also recites that limitation. That feature is shown, as one example, in Figure 6 of the present specification in which each of the trenches is parallel throughout the substrate. That feature clarified in independent Claim 7, and recited in new independent Claim 12, clearly distinguishes over the teachings in the applied art.

More specifically, in Figure 6 Okumura shows the use of trenches 16. However, those trenches 16 have curved or inclined portions in addition to parallel portions in a substrate. In contrast to that structure in Okumura, in the claimed invention the plurality of trenches are arranged substantially in parallel "throughout said semiconductor substrate". In such a way, the invention as recited in independent Claims 7 and 12, and the claims dependent therefrom, patentably distinguish over the teachings in Okumura. Moreover, no teachings in Kitagawa can overcome the above-noted deficiencies in Okumura in the above-discussed respect.

Independent Claim 7 has also been amended by the present response to clarify the first distance that the trenches are recessed, which corresponds as one example to distance L5

shown in Figure 10 of the present specification, and the alternate distance that the trenches are recessed, which corresponds to distance L6 shown in Figure 10 of the present specification. New independent Claim 12 also clarifies such distances.

The previous rejection of the claims took the position that such distances were disclosed in the applied art to Okumura. However, that position is traversed.

In Figure 5 of Okumura the center region having the N^+ diffused layer corresponds to the claimed distance L6, because the contact region is provided in this region. In Okumura the distance between trenches, which is located at the sides of the central region, corresponds to the claimed first distance L5. Therefore, in Okumura the relation between L5 and L6 is L5 < L6. That relation in Okumura is opposite to the claimed relation between the second and first distances.

In such ways, for such further reasons, the invention as recited in amended independent Claim 7 and new independent Claim 12, also patentably define over the teachings in Okumura. Moreover, no teachings in Kitagawa can overcome these further deficiencies of Okumura.

In view of these foregoing comments, the invention as recited in the currently pending Claims 7, 8, and 11-14 is allowable.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Registration No. 25,599
Attorney of Record
Surinder Sachar
Registration No. 34,423

22850
(703) 413-3000
Fax #: (703)413-2220
GJM:SNS/smi

I:\atty\SNS\00397207-pr.wpd

Marked-Up Copy
Serial No:
New Continuation App.
Amendment Filed on:
Herewith

IN THE CLAIMS

Please amend the claims as follows:

--Claims 1-6 (Canceled)

7. (Amended) An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof[;];

a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate and each recessed at a first distance (L5) and a second distance (L6) alternately, lower ends of said trenches extending to a depth extending from the surface of said semiconductor substrate to an upper portion of said N-type base layer;

a gate oxide layer provided on an inner surface of each of said trenches and on the surface of said semiconductor substrate;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate oxide layer and connected to said gate wire, with one set of said trench gate electrodes being constituted by twos arranged in sequence at the first distance (L5), and said first distance (L5) is greater than said second distance (L6);

an N-type emitter layer provided [on] in the surface part of [said semiconductor substrate of] said P-type base layer having a length of said second distance (L6) interposed

between said trench gate electrode belonging to said one set of electrodes and said trench gate electrodes belonging to another set of electrodes adjacent to said one set of electrodes, and in the vicinity of said trench gate electrode;

an insulating oxide layer provided covering a part or the whole of said trench gate electrode, and holed with contact holes at each of portions provided with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating oxide layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode provided on said P-type emitter layer on the underside of said semiconductor substrate;

wherein the predetermined depth of the trench is set to such an extent that a depletion layer formed extending from a top of said trench gate electrode when in a forward voltage application is fused with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is vicinal and that a curvature of said depletion layer at the top of said trench gate electrode is relieved.

Claims 9 and 10 (Canceled).

Claims 11-14 (New).--